Part I: Computer Architecture and Organization (50%)

1. (a) The history of computers is divided into three generations. What are the three generations? (2%)

   (b) What are the important concepts of a "von Neumann Machine"? (2%)

   (c) What is the "Moore's Law"? (2%)

   (d) The instruction format of a simple machine is shown below:

0 Opcode 7	8 Address 23

   i. What is the maximum memory address space that a processor can access directly? (2%)

   ii. What is the maximum memory capacity if the machine has 16-bit data bus? (2%)

2. Assume a simple machine is listed as follows.

Instruction format	0 Opcode 3	4 Address 15

The opcodes are defined as follows:

Opcode	Meaning
1	Load AC from memory
2	Store AC to memory
5	Add to AC from memory

A program of three instructions is shown below:

1. Load AC from memory location 689 (hex value)
2. Add to AC from memory location 690
3. Store AC to memory location 691

Please list the above program in hex value. (5%)

3. (a) Please explain the mechanism of DMA. (3%)

   (b) Two DMA configurations are shown on Figure 1. Which one has a higher transfer rate? Why? (3%)

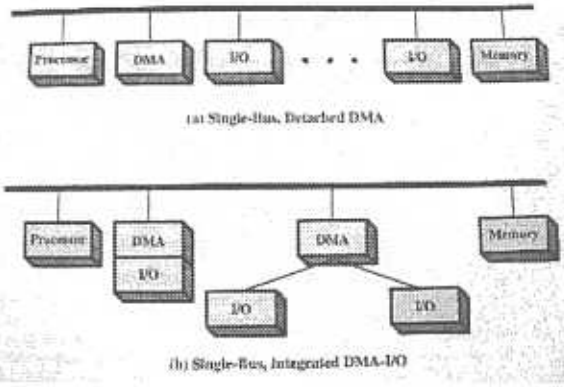

Figure 1

4. (a) Why Booth's algorithm is designed for 2's complement multiplication? (3%)

   (b) Please compute 01011×11001 with Booth's algorithm. (5%)

5. Assume the format of address for a 2-way set associative mapping cache is shown below and each word is 64 bits.

Tag: 16 bits	Set: 10 bits	Word: 5 bits

(a) What size is the main memory? (3%)

(b) What size is the cache? (3%)

6. Please explain the concept of "register windows" used in RISC computers. (5%)

7. If an instruction processing can be decomposed into the following stages:

FI: fetch instruction

DI: decode instruction

CO: calculate operands

FO: fetch operands

EI: execute instruction

WO: write operand

(a) Please use a timing diagram to explain the concept of "pipelining." (4%)

(b) What is the influence of branch instructions on pipelining? How to deal with branches? (6%)

PartII: Operating System (50%)

8. Supposed that the LRU page-replacement algorithm is implemented.

(a) Explain what is LRU page-replacement algorithm. (2%)

(b) If the 4 frames are initially empty, how many page faults occur for the following reference string, if the LRU algorithm is applied? (5%)

1, 2, 3, 4, 5, 6, 4, 5, 8, 7, 4, 5, 1, 4, 5, 8,7

9. Please explain what is thrashing. (2%)What is working set? (2%) What is the relationship between thrashing and working set? (2%)

10. What is deadlock? (2%) Please list and explain the necessary conditions when the deadlock occurs. (4%) Please explain how to avoid the deadlock condition. (4%)

11. For the processes shown in the box, what is the average waiting time using:
    (a) The Short-Job-First scheduling? (3%)
    (b) The First-Come-First-Serve scheduling? (3%)
    (c) The Round-Robin scheduling with a quantum = 10ms? (4%)

Process	Burst（ms）
P1	20
P2	28
P3	5
P4	8
P5	18

12. What is spooling? (2%)Please illustrate an example using the spooling method to solve problems? (3%)
13. Please answer the following questions.
    (a) What is critical section? (2%)
    (b) What if one of cooperative processes has incorrect use of semaphore as following? Explain your answer. (3%)

```
wait(s)
critical section
wait(s)
```

    (c) The following is an incorrect solution of using Test-and-Set to implement the semaphore operations wait(s) and signal(s). Please show why it is incorrect. (7%)

```
procedure wait(s)
  begin
    while Test-and-Set(lock) do no-op;
    while(s≦0) do no-op;
    s = s-1;
    lock = free;
  end;
procedure signal(s)
  begin
    while Test-and-Set(lock) do no-op;
    s = s + 1;
    lock = false;
  end;
```