1. Processes frequently need to communicate with other processes. For example, in a shell pipeline, the output of the first process must be passed to the second process, and so on down the line. In the issues of InterProcess Communication (IPC), what is a race condition? And, please explain the difference between busy waiting and blocking. (12%) 

2. A computer has four frames. The time of loading, time of last access, and the R and M bits for each page are shown below (the times are in clock ticks): (8%) 

<table>
<thead>
<tr>
<th>Page</th>
<th>Loaded</th>
<th>Last ref.</th>
<th>R</th>
<th>M</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>126</td>
<td>279</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>230</td>
<td>260</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>120</td>
<td>272</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>160</td>
<td>280</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

(a) Which page will NRU replace?  
(b) Which page will FIFO replace?  
(c) Which page will LRU replace?  
(d) Which page will second chance replace?  

3. State the four necessary conditions for a deadlock to exist. Give a brief intuitive argument for the reason each individual condition is necessary. (10%)  

4. Use tree height reduction techniques to produce versions of the following expressions more amenable to parallel evaluation. In each case draw evaluation trees for the original expression and the new expression. (8%)  

(a) \((p+(q+(r+s)))\)  
(b) \(((a+b*c*d)*e)\)  
(c) \((m+(n*p*q*r)+a+b+c)\)  
(d) \((a*(b+c)+d*(e+f))\)
5. Compare and contrast the notions of peer-to-peer network architecture and hierarchical network architecture. Which is better for network management? Which offers great flexibility in resource sharing? Why do you suppose most OSI relationships are peer-to-peer? (12%)
6. (8%) Proper noun explanation: Please explain the following terms. You must clearly describe their meaning and purpose.
   (A) Hard-wired program
   (B) Bus arbiter
   (C) Demand paging
   (D) PCB (Process Control Block)

7. (6%) What is the most important concept of a “von Neumann Machine”?

8. (6%) What is a SEC-DED code? If there is a 4-bit data word, please explain by an example how the code works when two errors occur.

9. (6%) Consider a machine with a byte addressable main memory of 1M bytes and block size of eight bytes. Assume the cache is 16K bytes. Answer the following questions:
   (A) If the cache is direct mapping cache, how is the address divided into fields to determine a cache hit/miss?
   (B) If the cache is a four-way set associative mapping cache, how is the address divided into fields to determine a cache hit/miss?

10. (4%) (A) What are the three basic I/O techniques? (B) Which one uses “cycle stealing’’?

11. (5%) A PC-relative mode branch instruction is stored in memory at address 236₁₀. The branch is made to location 327₁₀. The address field in the instruction is 12 bits long. What is the binary value of address field in the branch instruction?

12. (5%) (A) Please compute 1010 × 0110 with Booth’s algorithm.

13. (10%) A register interference graph is shown at the right-hand side and graph-coloring approach is used to assign these nodes into three registers (R1, R2, R3) or memory. Please answer the best case.